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CUSTOMER NO.
48744

27. (Original) The BIOS memory of claim 22 wherein said second set of instructions further causes said boot strap processor to communicate said initial configuration to said plurality of processing nodes over the array.

REMARKS

Claims 1-27 remain present in this application. In the present Office action: claim 4 was objected to; claims 9, 10, 12, and 14 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,327,548 (hereinafter Hardell); claims 1-3, 5, 6, and 8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hardell in view of U.S. Patent No. 5,740,349 (hereinafter Hasbun); claim 13 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hardell in view of Hasbun; claims 16-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hardell in view of Hasbun and U.S. Patent No. 6,571,347 (hereinafter Tseng); claims 22-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hardell in view Tseng; and claims 4, 7, 11, 15, 20, 21, 26, and 27 were indicated to be allowable if rewritten in independent form. Applicant wishes to extend appreciation to the Examiner for the indication of allowable subject matter. However, for at least the reasons set forth below, Applicant submits that all of claims 1-27 are now allowable over the applied prior art. Applicant has amended claims 1 and 16 and has made minor clarifying amendments to claims 4, 5, and 14.

With respect to independent claim 1, Applicant respectfully submits that while Hardell discloses a system that includes multiple processing nodes, neither Hardell or Hasbun, alone or in combination, teach or suggest a method of testing memory that determines a configuration of an array of processing nodes. Moreover, Applicant notes that none of the Hardell processing nodes are directly coupled to another of the Hardell processing nodes. Furthermore, Hardell does not disclose how a configuration of an array of processing nodes could be determined and presumably has the array configuration pre-programmed. Additionally, Hasbun is not directed to a multiprocessor system. With reference to Applicant's specification (see Fig. 2), an example is provided as to how a configuration of processing nodes may be determined. More specifically, at paragraph [0038], "[d]uring POST 420, BSP 210 performs an HT map task 422 by detecting the presence and interconnection of the installed processor nodes. The HT map takes the form of a routing table that the BIOS provides to all nodes, and in this way the BIOS configures the HT

fabric." Applicant notes that Hardell is directed to implementation of spare bit steering (spare bits are used to replace bad data bits). Applicant also notes that a global memory spare bit steering configuration is distributed to processors of the Hardell system via commonly accessible register(s) of an atomic semaphore controller or through a commonly accessible block of global memory (see, for example, the Hardell Abstract). While of different scope, Applicant's independent claims 16 is also allowable for substantially the same reasons set forth above with respect to claim 1, as neither Hardell, Hasbun or Tseng, alone or in combination, teach or suggest a set of instructions that determines a configuration of an array of processing nodes.

With respect to independent claim 9, Applicant respectfully submits that while Hardell includes multiple processing nodes and global memory, the global memory of Hardell is not configured by programming a plurality of processing nodes with an initial configuration. As noted above, the Hardell system provides processor access to a global memory spare bit steering configuration via commonly accessible register(s) of an atomic semaphore controller or through a commonly accessible block of global memory. This does not teach configuring a distributed memory by programming a plurality of processing nodes with an initial configuration. Additionally, Applicant notes that the Examiner's rejection of claim 9 appears to be inconsistent with the position taken with respect to Applicant's claim 21, which is directed to communicating an initial memory configuration to a plurality of processing nodes. While of different scope, Applicant's independent claim 22 is also allowable for substantially the same reasons set forth above with respect to claim 9, as neither Hardell or Tseng, alone or in combination, teach or suggest configuring a memory by programming a plurality of processing nodes with an initial configuration. Furthermore, Applicant submits that claims 2-8, 10-15, 17-21, and 23-27 are also allowable for at least the reason that the claims depend upon allowable claims.

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CONCLUSION

Applicant respectfully submits that the present application is now in condition for allowance. Accordingly, the Examiner is requested to issue a Notice of Allowance for all pending claims. Should the Examiner deem that any further action by the Applicant would be desirable for placing this application in even better condition for issue, the Examiner is requested to telephone Applicant's undersigned representative at the number listed below.

Applicant does not believe that any additional fees are due, but if the Commissioner believes additional fees are due, the Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 01-0365.

Respectfully submitted,

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Date

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